AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF THE CLAIMS:

Claims 1-12 (cancelled)

13. (withdrawn) A semiconductor device comprising:

a semiconductor chip which includes bonding pads arranged along at least a first side and a second side which faces the first side in an opposed manner; and

a package substrate which includes bonding leads formed corresponding to the first side and the second side of the semiconductor chip and external terminals connected to the bonding leads,

wherein the bonding leads have portions thereof over which wires connected to other bonding leads pass notched.

14. (withdrawn) A semiconductor device comprising:

a semiconductor chip including bonding pads which are arranged along at least a first side and a second side which faces the first side in an opposed manner; and

a package substrate including bonding leads which are formed corresponding to the first side and the second side

of the semiconductor chip and external terminals which are connected to the bonding leads,

wherein the bonding leads are arranged in a staggered manner at two inner and outer rows along the extension direction of wires which are connected to the bonding leads,

wherein the pull-out direction of wiring layers leading to respective lead through-holes are directed toward the inside of the package substrate, and

wherein notched portions are formed in inner ends of the inside bonding leads at the two inner rows.

15. (New) A semiconductor device comprising:

a memory chip including first bonding pads for address arranged along a first side of the memory chip, and second bonding pads for data arranged along a second side which faces the first side in an opposed manner;

a package substrate including first bonding leads arranged along a first side of the package substrate corresponding to the first side of the memory chip, and second bonding leads arranged along a second side of the package substrate corresponding to the second side of the memory chip;

a semiconductor chip including third bonding pads arranged along a first side thereof, an address output circuit, fourth bonding pads arranged along a second side

thereof which faces the third side in an opposed manner, a data input/output circuit which serves for memory access, and a signal processing circuit having a data processing function,

wherein the first and third bonding pads are connected in common to the first bonding leads of the package substrate and the second and fourth bonding pads are connected in common to the second bonding leads of the package substrate, and

wherein the memory chip and the semiconductor chip are mounted on the package substrate in a stacked structure.

16. (new) A semiconductor device according to claim 15, wherein wires are used to connect said first and third bonding pads to said first bonding leads and to connect said second and fourth bonding pads to said second bonding leads.

17. (new) A semiconductor device according to claim 15,

wherein the first and second bonding pads are arranged with a correspondence to pitches of the third and fourth bonding pads, respectively, and

wherein fifth and sixth bonding pads are independently formed along opposing sides of the

semiconductor chip between said first and second bonding pads.

18. (new) A semiconductor device according to claim 15, wherein the package substrate includes first wiring layers on a front surface thereof on which the memory chip is mounted, and second wiring layers on a back surface thereof on which balls constituting external terminals are formed, and the first wiring layers are connected to corresponding second wiring layers via through-holes.

19. (new) A semiconductor device according to claim 18,

wherein the semiconductor chip constitutes a one chip microcomputer, and

wherein bonding pads on third and fourth sides of the semiconductor chip are electrically connected to respective ones of said external terminals.

20. (new) A semiconductor device according to claim 19,

wherein the memory chip has an area larger than an area of the semiconductor chip and is formed into a rectangular shape in which a length of the first side and

the second side is shorter than a length of two other sides, and

wherein directions of wires of the first wiring layers leading from said first and second bonding leads to the through-holes are arranged to extend toward an inner region of the package substrate.

21. (new) A semiconductor device according to claim 20,

wherein the semiconductor chip is mounted on a surface of the memory chip so as to provide a stacked structure.

22. (new) A semiconductor device according to claim 19, wherein the package substrate has third and fourth bonding leads arranged respectively along third and fourth sides of the package substrate, and directions of wires of the first wiring layers leading from the third bonding leads to through-holes are distributed toward the inner region and an outer region of the package substrate relative to the third bonding leads, and directions of wires of the first wiring layers leading from the fourth bonding leads to through-holes are distributed toward the inner region and the outer region of the package substrate relative to the fourth bonding leads.

23. (new) A semiconductor device according to claim 22, wherein said third and fourth bonding leads are shorter in length than said first and second bonding leads.

24. (new) A semiconductor device according to claim 20, wherein at least some of the first bonding leads and the second bonding leads are formed into rectangular configuration such that longitudinal directions of those first bonding leads are substantially aligned with extension directions of wires which connect those first bonding leads with corresponding first and third bonding pads, and longitudinal directions of those second bonding leads are substantially aligned with extension directions of wires which connect those second bonding leads with corresponding second and fourth bonding pads.

25. (new) A semiconductor device according to claim 21, wherein said first and second bonding leads include bonding leads having notched portions over which wires connected to other bonding leads pass.

26. (new) A semiconductor device according to claim 24,

wherein said first and second bonding leads are arranged in a staggered manner, each in two inner and outer rows along extension directions of wires which are connected thereto, and

wherein notched portions are formed at inner ends of bonding leads in said inner rows.